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## Claims

We claim:

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1. A method of processing an interrupt verification support mechanism in a computer system comprising a processor and an input for external interrupts communicatively coupled to the processor, the method comprising the steps:

(a) processing at least one actual instruction in the processor; and

15 (b) if an external interrupt request or an interrupt pseudo-instruction is received by the processor, the actual instruction is replaced with the pseudo-instruction.

2. The method of claim 1 comprising :

20 processing at least one actual instruction in the processor in an instruction pipeline wherein instructions are processed concurrently by an instruction fetch stage, an instruction decode stage, an instruction issue stage, an instruction execute stage and a result write-back stage.

3. The method of claim 1 comprising :

25 if an external interrupt request or an interrupt pseudo-instruction is received by the processor, replacing the actual instruction present in the instruction fetch stage with the pseudo-instruction.

4. The method of claim 1 further comprising:

30 creating the pseudo-instruction by a co-processor connected to the processor.

5. The method of claim 1 comprising:

35 simultaneously processing a number of instructions in the processor in an instruction pipeline with several instruction stages each instruction being in a different instruction stage at a time.

6. The method of claim 1 further comprising:

5 storing at least the information of the program counter of the instruction which is to be interrupted and the sort of interrupt to use in a set of one or more interrupt registers of the processor.

7. The method of claim 1 further comprising:

10 comparing the data content of a program counter with the data content of an interrupt register and replacing the actual instruction with a pseudo-instruction when the data content of the program counter matches the data content of the interrupt register, or when an external interrupt is present.

15 8. Interrupt verification support mechanism device for a computer system comprising a processor and an input for external interrupt requests or interrupt pseudo-instructions communicatively coupled to the processor, wherein the device includes a set of one or more interrupt registers each of which contains information, at least the program counter of the instruction which is to be interrupted and the sort of interrupt to use, so as to enable  
20 the device to process at least one actual instruction, and if an external interrupt request is received by the processor, the actual instruction is replaced with the pseudo-instruction.

9. The device of claim 8 wherein  
the device further comprises an instruction fetch with a program counter and an interrupt  
25 register, the instruction fetch being coupled to a first input of a de-multiplexer for transmitting instructions to said de-multiplexer, the second input of the de-multiplexer connected to an interrupt pseudo-instruction input and the program counter connected with the interrupt register by a comparator.

30 10. The device of claim 9 wherein  
the second input of the de-multiplexer is capable of receiving interrupt pseudo-instruction signals or external interrupt requests.

11. The device of claim 9 wherein  
35 the comparator creates a high level signal only if the data content of the program counter matches the data content of the interrupt register.

12. The device of claim 9 wherein

5 the output of the comparator is connected to the first input of an or-operator, and the second input of the or-operator is connected to an interrupt controller so as to enable the or-operator to create a high level signal if the signal received from the interrupt controller differs from the signal received from the comparator.

10 13. The device of claim 9 wherein, when the data content of the program counter matches the data content of the interrupt register, the actual instruction is replaced with a pseudo-instruction.

14. The device of claim 9 wherein  
15 when an external interrupt request is present at the de-multiplexer, the actual instruction is replaced with an interrupt pseudo-instruction.

15. The device of claim 9 wherein  
the instruction coming from the output of the de-multiplexer is sequentially processed in  
20 the instruction pipeline of the processor.

16. The device of claim 9 wherein  
the instruction pipeline of the processor includes an instruction fetch stage, an instruction  
decode stage, an instruction issue stage, an instruction execute stage and a result write-  
25 back stage.

17. The device of claim 9 wherein  
the interrupt pseudo-instruction effects the instruction state stages required by the  
interrupt.

30 18. The device of claim 16 wherein  
if an interrupt request or an interrupt pseudo-instruction is received by the processor, the processor is adapted to cancel an instruction that is in the instruction fetch stage when the interrupt request or the interrupt pseudo-instruction is received and to reissue the  
35 instruction starting at the instruction fetch stage.

19. The device of claim 16 wherein

- 5 if an interrupt request or an interrupt pseudo-instruction is received by the processor, the processor is adapted to cancel an instruction that is in any instruction stage when the interrupt request or the interrupt pseudo-instruction is received and to reissue the instruction starting at the instruction fetch stage.
- 10 20. The device of claim 8 wherein the pseudo-instruction is created by a co-processor connected to the processor.
21. The device of claim 8 wherein the device is a media decoding system, the processor is a core decoder processor and  
15 the co-processor is a decoding accelerator adapted to assist the core processor with a decoding function.
22. The device of claim 20 wherein the processor is a reduced instruction set computer (RISC) processor.
- 20 23. A computer comprising the device of claim 8.
24. A computer utilizing the method of claim 1.